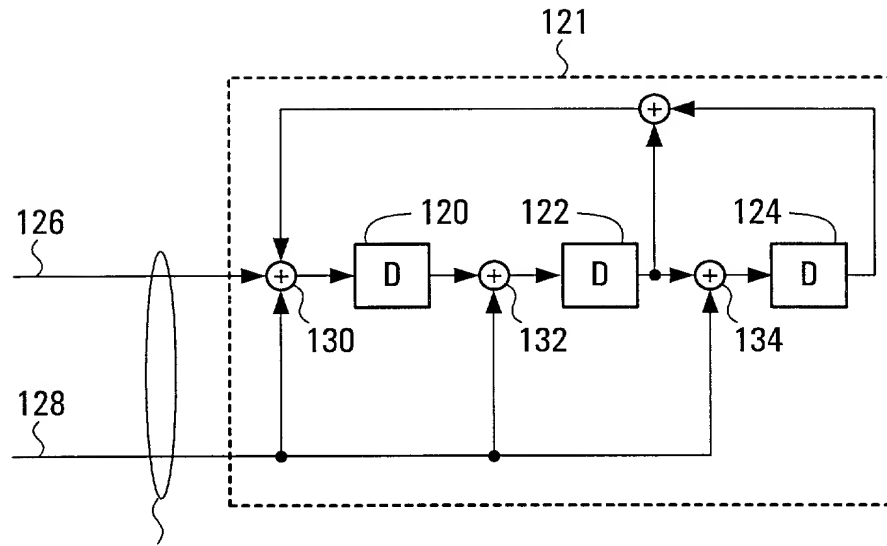


FIG. 1



TWO INPUT BITS PER STATE
TRANSITION INTERVAL

FIG. 2

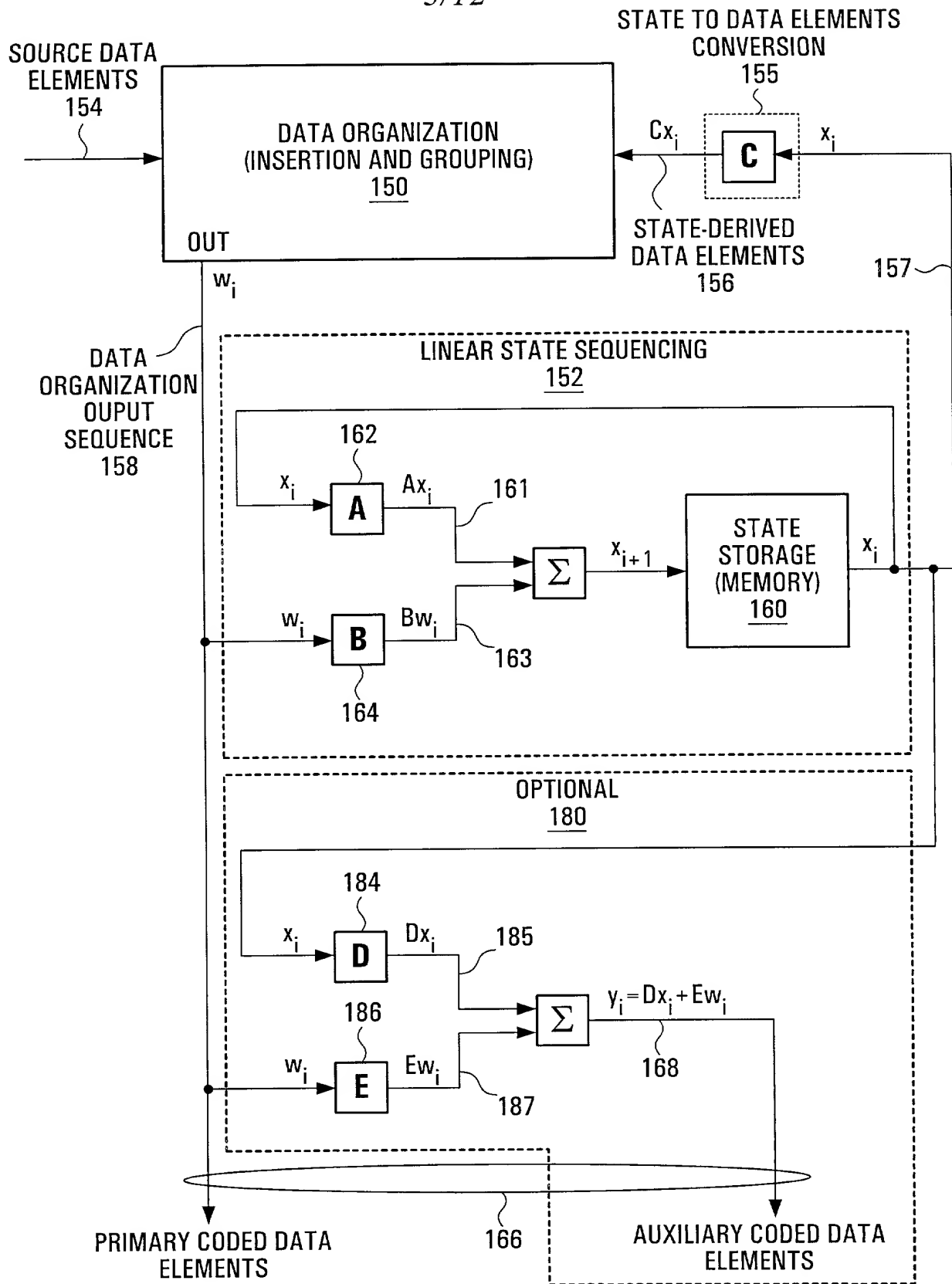


FIG. 3

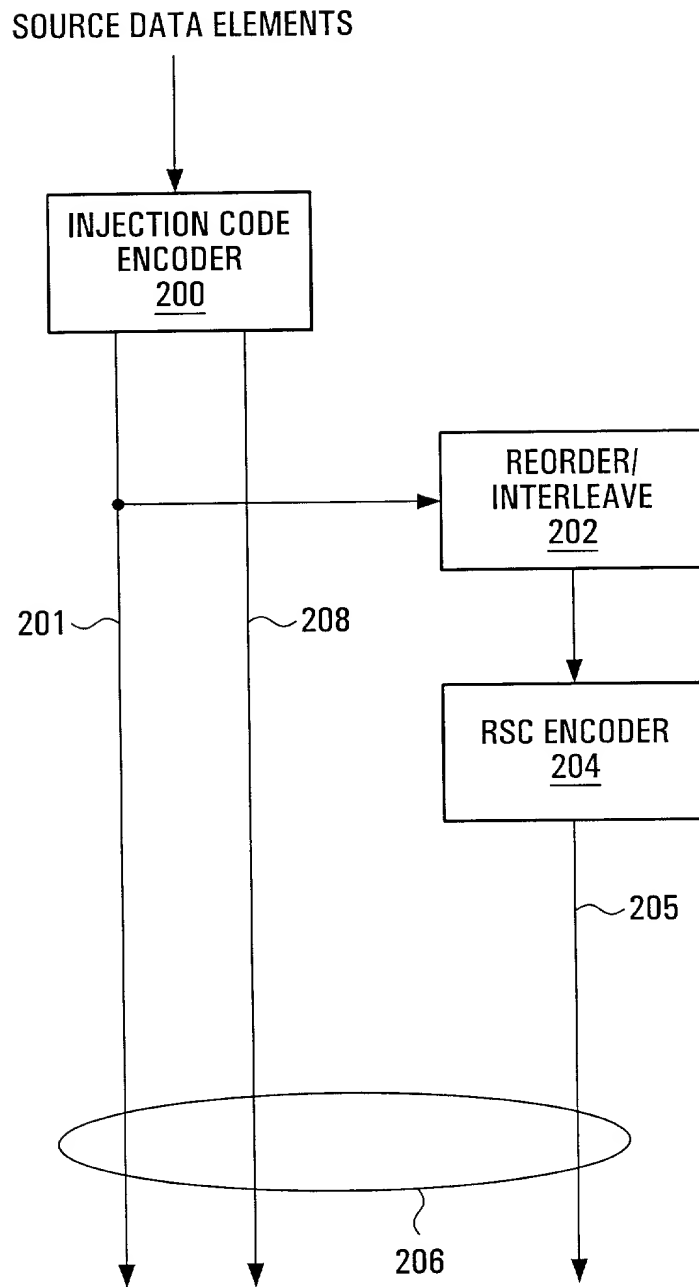


FIG. 4

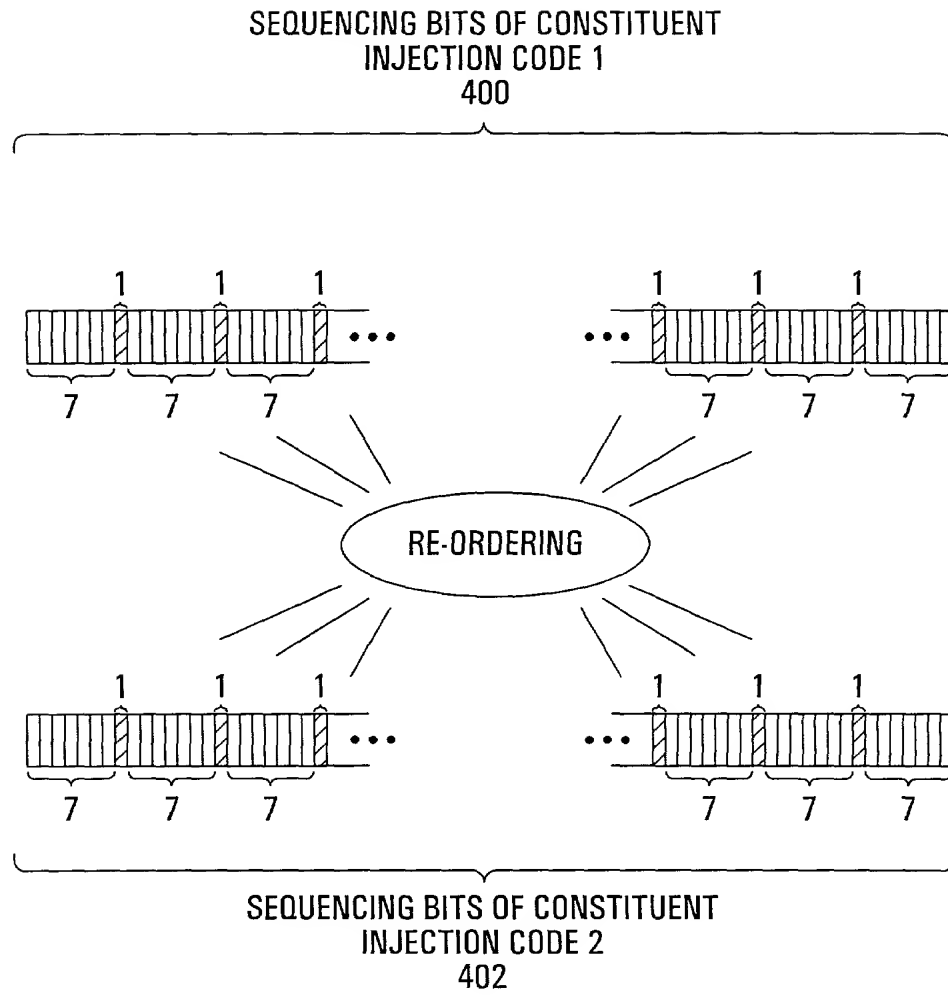


FIG. 5

FIG. 7

FIG. 7

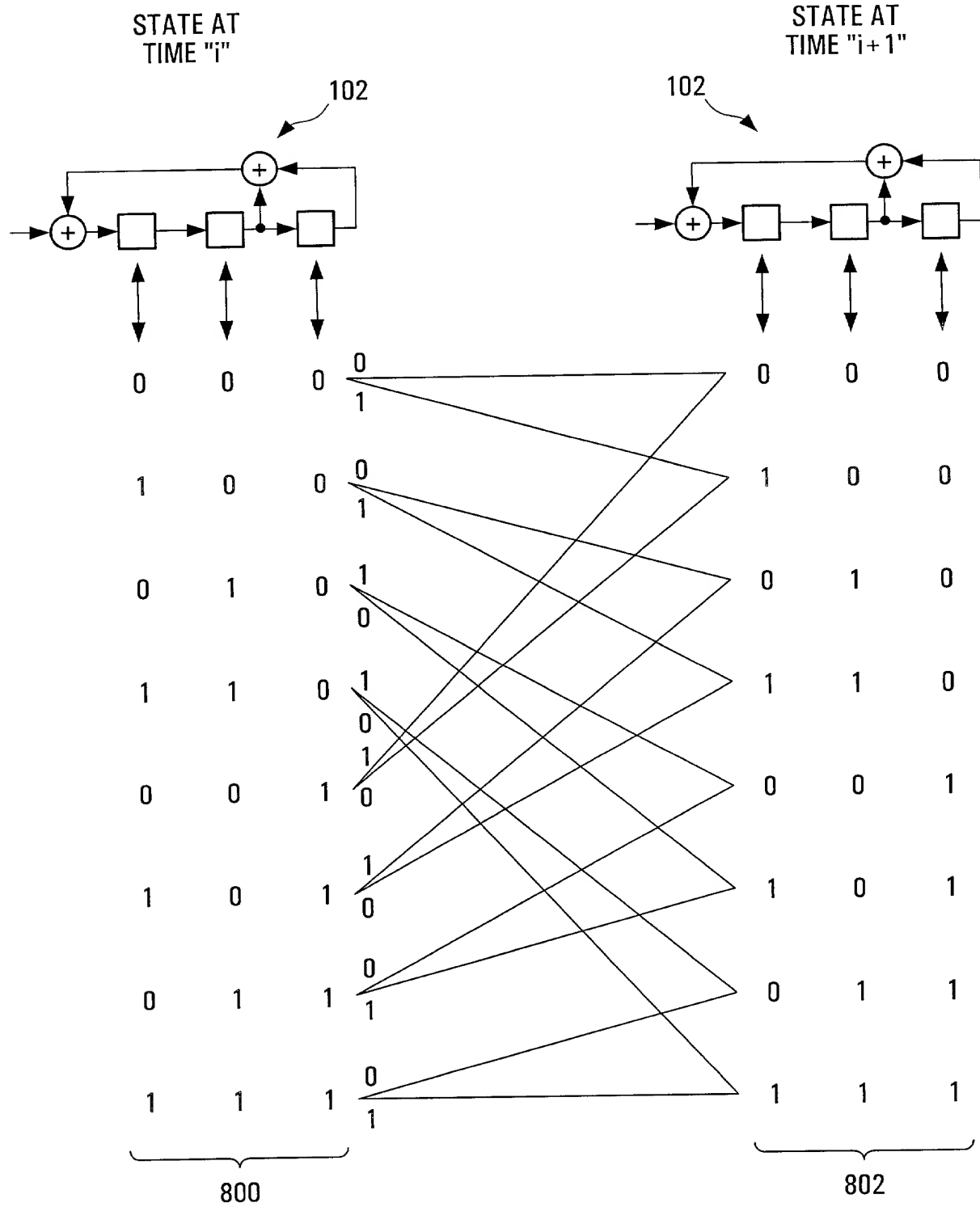


FIG. 8A

9/12

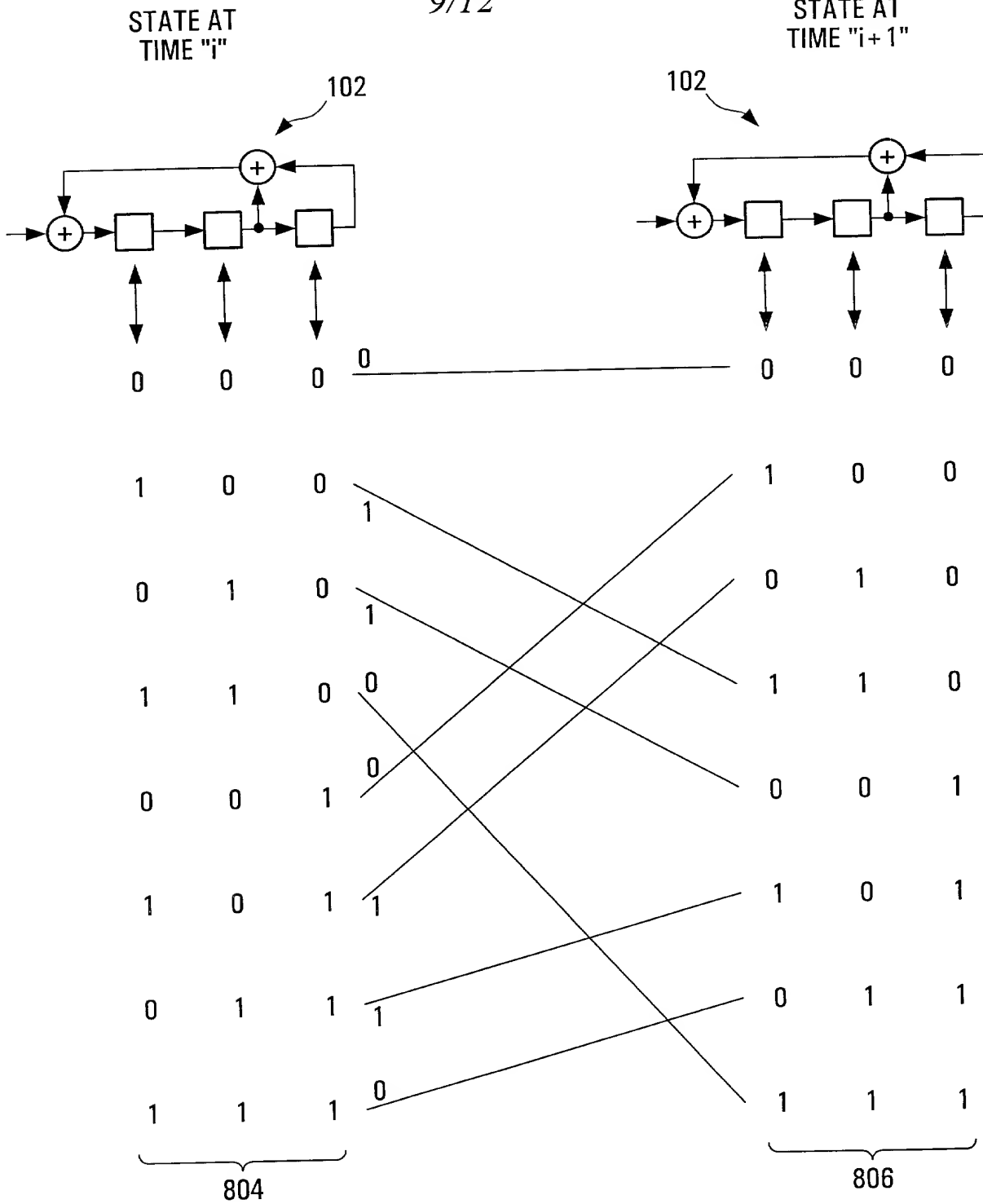


FIG. 8B

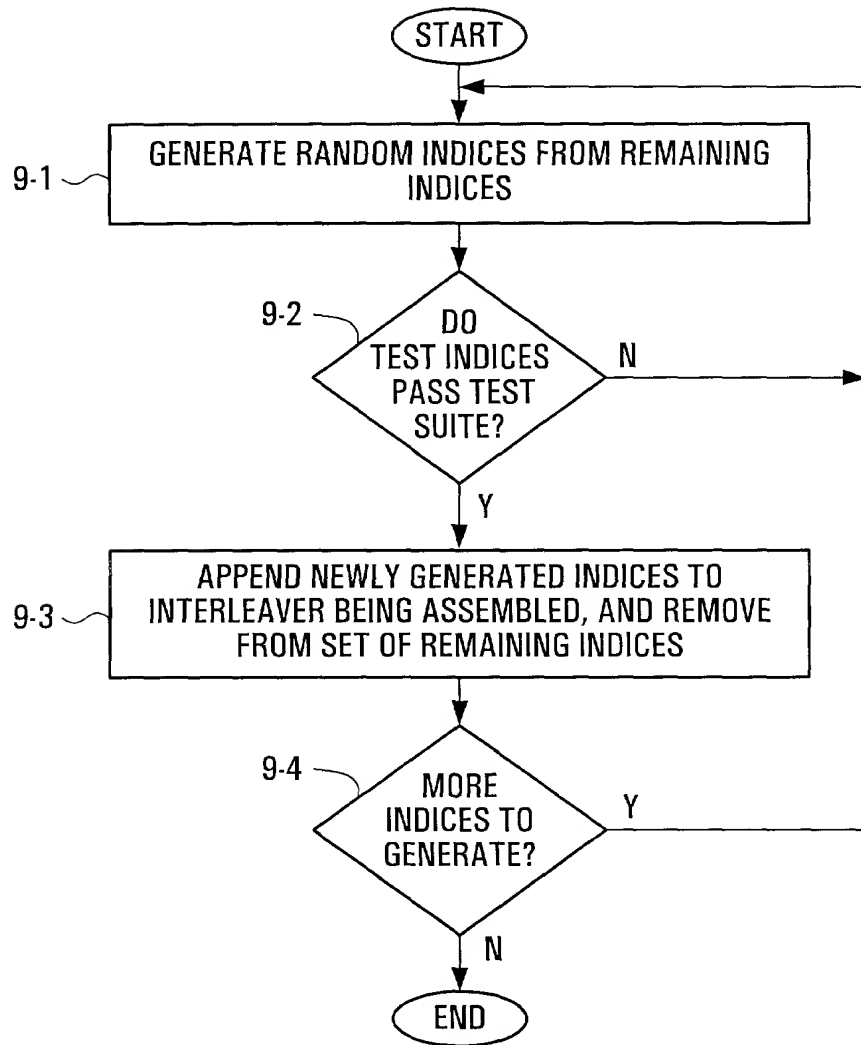


FIG. 9

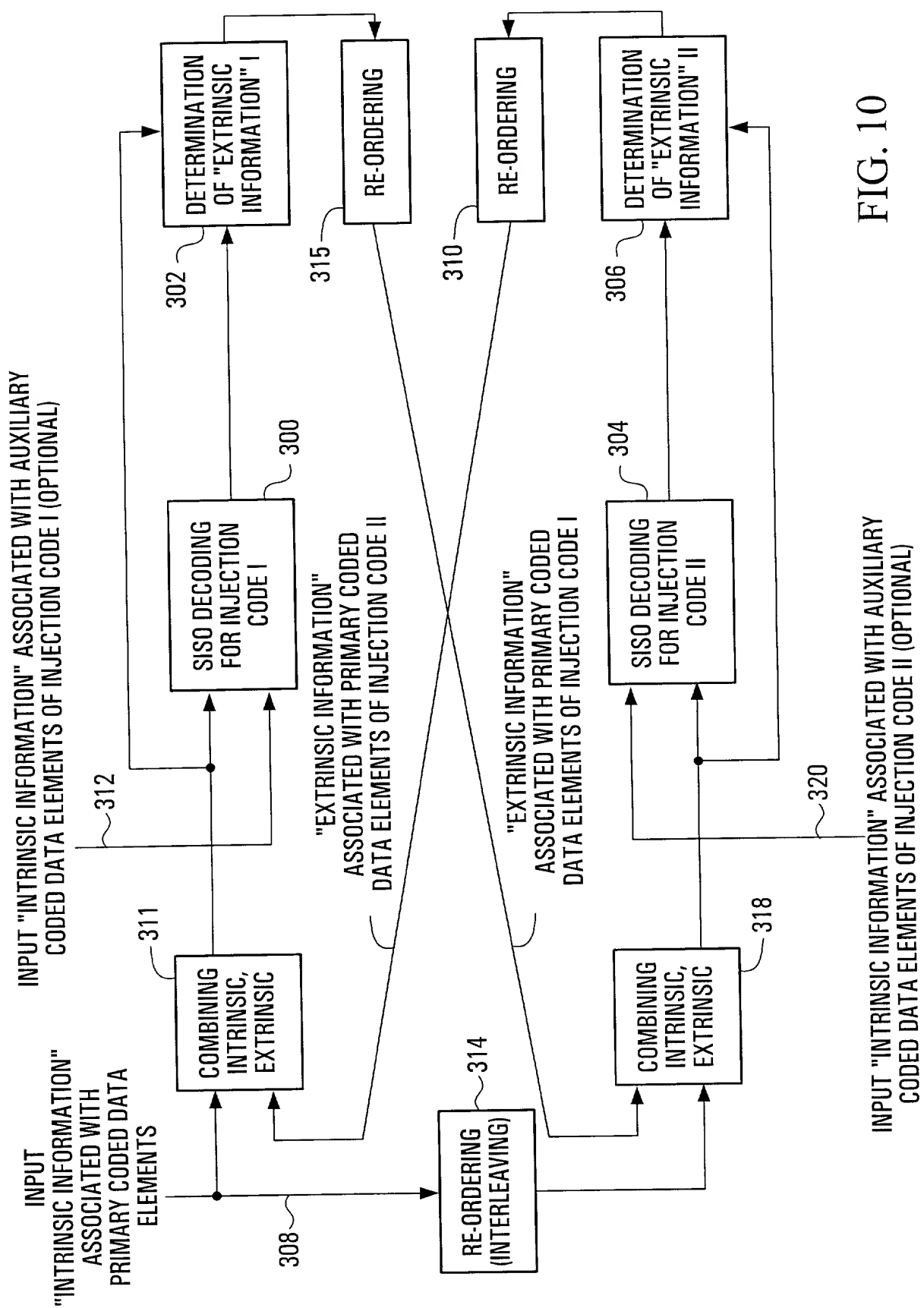


FIG. 10

FIG. 11

